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FAIRCHILD SEMICONDUCTOR™

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# DM74LS90
# Decade and Binary Counters

## General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the DM74LS90.

All of these counters have a gated zero reset and the DM74LS90 also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade or four bit binary), the B input is connected to the $Q_A$ output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the DM74LS90 counters by connecting the $Q_D$ output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output $Q_A$.

## Features

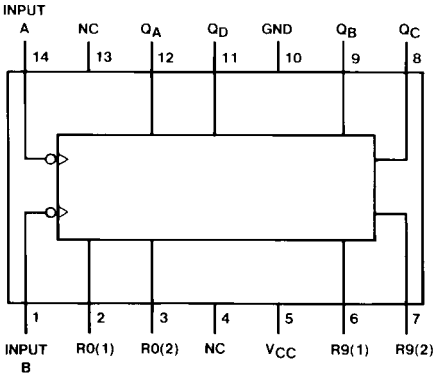
- Typical power dissipation 45 mW
- Count frequency 42 MHz

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| DM74LS90M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow |
| DM74LS90N | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagram




## Reset/Count Truth Table

| Reset Inputs | | | | Output | | | |
|---|---|---|---|---|---|---|---|
| R0(1) | R0(2) | R9(1) | R9(2) | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | X | L | L | L | L |
| H | H | X | L | L | L | L | L |
| X | X | H | H | H | L | L | H |
| X | L | X | L | COUNT | | | |
| L | X | L | X | COUNT | | | |
| L | X | X | L | COUNT | | | |
| X | L | L | X | COUNT | | | |

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## Function Tables

**BCD Count Sequence** (Note 1)

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

**Bi-Quinary (5-2)** (Note 2)

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_A$ | $Q_D$ | $Q_C$ | $Q_B$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

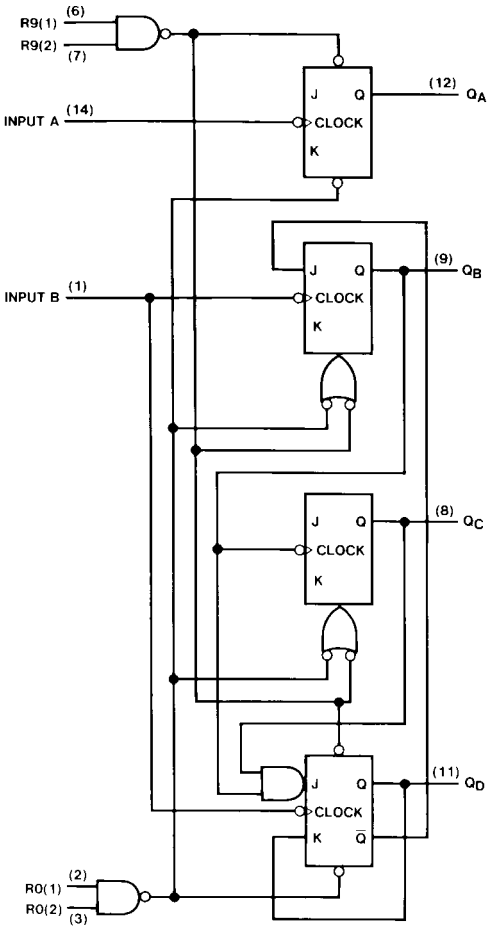
H = HIGH Level
L = LOW Level
X = Don't Care

**Note 1:** Output $Q_A$ is connected to input B for BCD count.

**Note 2:** Output $Q_D$ is connected to input A for bi-quinary count.

**Note 3:** Output $Q_A$ is connected to input B.

## Logic Diagram




The J and K inputs shown without connection are for reference only and are functionally at a high level.

## Absolute Maximum Ratings(Note 4)

| | |
|---|---|
| Supply Voltage | 7V |
| Input Voltage (Reset) | 7V |
| Input Voltage (A or B) | 5.5V |
| Operating Free Air Temperature Range | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |

**Note 4:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | | Min | Nom | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | HIGH Level Input Voltage | | 2 | | | V |
| $V_{IL}$ | LOW Level Input Voltage | | | | 0.8 | V |
| $I_{OH}$ | HIGH Level Output Current | | | | −0.4 | mA |
| $I_{OL}$ | LOW Level Output Current | | | | 8 | mA |
| $f_{CLK}$ | Clock Frequency (Note 5) | A to $Q_A$ | 0 | | 32 | MHz |
| | | B to $Q_B$ | 0 | | 16 | |
| $f_{CLK}$ | Clock Frequency (Note 6) | A to $Q_A$ | 0 | | 20 | MHz |
| | | B to $Q_B$ | 0 | | 10 | |
| $t_W$ | Pulse Width (Note 5) | A | 15 | | | ns |
| | | B | 30 | | | |
| | | Reset | 15 | | | |
| $t_W$ | Pulse Width (Note 6) | A | 25 | | | ns |
| | | B | 50 | | | |
| | | Reset | 25 | | | |
| $t_{REL}$ | Reset Release Time (Note 5) | | 25 | | | ns |
| $t_{REL}$ | Reset Release Time (Note 6) | | 35 | | | ns |
| $T_A$ | Free Air Operating Temperature | | 0 | | 70 | °C |

**Note 5:** $C_L$ = 15 pF, $R_L$ = 2 kΩ, $T_A$ = 25°C and $V_{CC}$ = 5V.

**Note 6:** $C_L$ = 50 pF, $R_L$ = 2 kΩ, $T_A$ = 25°C and $V_{CC}$ = 5V.

## Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | | Min | Typ (Note 7) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | −1.5 | V |
| $V_{OH}$ | HIGH Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = Max, $V_{IL}$ = Max, $V_{IH}$ = Min | | 2.7 | 3.4 | | V |
| $V_{OL}$ | LOW Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = Max, $V_{IL}$ = Max, $V_{IH}$ = Min | (Note 8) | | 0.35 | 0.5 | V |
| | | $I_{OL}$ = 4 mA, $V_{CC}$ = Min | | | 0.25 | 0.4 | |
| $I_I$ | Input Current @ Max Input Voltage | $V_{CC}$ = Max, $V_I$ = 7V | Reset | | | 0.1 | mA |
| | | $V_{CC}$ = Max, $V_I$ = 5.5V | A | | | 0.2 | |
| | | | B | | | 0.4 | |
| $I_{IH}$ | HIGH Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7V | Reset | | | 20 | µA |
| | | | A | | | 40 | |
| | | | B | | | 80 | |
| $I_{IL}$ | LOW Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4V | Reset | | | −0.4 | mA |
| | | | A | | | −2.4 | |
| | | | B | | | −3.2 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (Note 9) | | −20 | | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (Note 7) | | | 9 | 15 | mA |

**Note 7:** All typicals are at $V_{CC}$ = 5V, $T_A$ = 25°C.

## Electrical Characteristics (Continued)

**Note 8:** $Q_A$ outputs are tested at $I_{OL}$ = Max plus the limit value of $I_{IL}$ for the B input. This permits driving the B input while maintaining full fan-out capability.

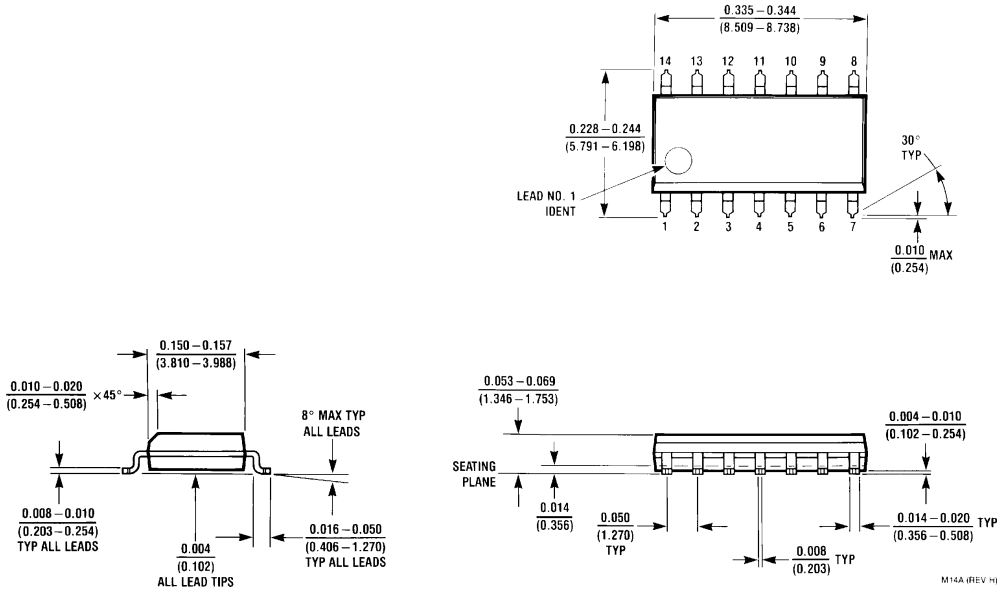
**Note 9:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

**Note 10:** $I_{CC}$ is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

## Switching Characteristics at $V_{CC}$ = 5V and $T_A$ = 25°C

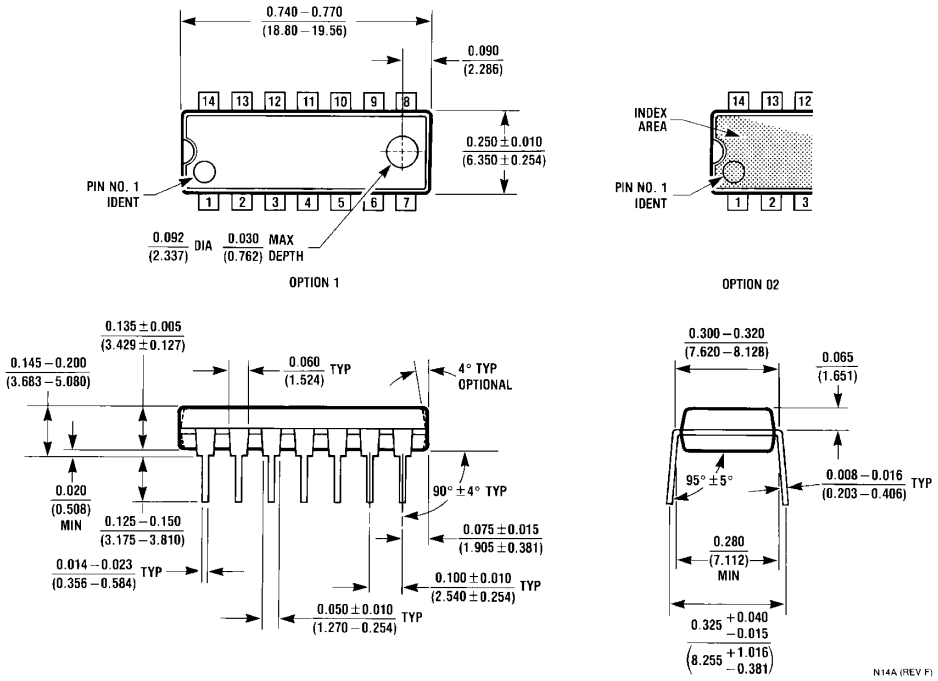
| Symbol | Parameter | From (Input) To (Output) | $R_L$ = 2 kΩ | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | $C_L$ = 15 pF | | $C_L$ = 50 pF | | |
| | | | Min | Max | Min | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | A to $Q_A$ | 32 | | 20 | | MHz |
| | | B to $Q_B$ | 16 | | 10 | | |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | A to $Q_A$ | | 16 | | 20 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | A to $Q_A$ | | 18 | | 24 | ns |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | A to $Q_D$ | | 48 | | 52 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | A to $Q_D$ | | 50 | | 60 | ns |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | B to $Q_B$ | | 16 | | 23 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | B to $Q_B$ | | 21 | | 30 | ns |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | B to $Q_C$ | | 32 | | 37 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | B to $Q_C$ | | 35 | | 44 | ns |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | B to $Q_D$ | | 32 | | 36 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | B to $Q_D$ | | 35 | | 44 | ns |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | SET-9 to $Q_A$, $Q_D$ | | 30 | | 35 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | SET-9 to $Q_B$, $Q_C$ | | 40 | | 48 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | SET-0 to Any Q | | 40 | | 52 | ns |

## Physical Dimensions inches (millimeters) unless otherwise noted




**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow**
**Package Number M14A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide**
**Package Number N14A**

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